

MODELING CARBON NANOTUBE VIAS

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Carbon nanotubes (CNTs) are innovative materials proposed to replace conventional metals to fabricate interconnects for nanoelectronics [1]. Theoretical studies have shown that CNT interconnects can overcome copper ones in electrical and thermal performances for nanoscale technology nodes [2]-[3]. In the meanwhile, the rapid progress in CNT fabrication has made possible the first examples of CNT interconnects [4], of CNT-based vias and pillars [5] and of CNT Through Silicon Vias [6].

To realize vertical interconnects able to meet the tight requirements of the future nanoelectronic technologies [7], bundles of either single-walled carbon nanotubes (SWCNTs) or multi-walled carbon nanotubes (MWCNTs) are proposed. As CNT interconnects move from a research area to real-world applications, more sophisticated models are needed to describe typical operating conditions. To analyze the problem of integrating CNT and CMOS technologies it is compulsory to take into account effects that have a major impact on the electrical parameters: the geometrical size, the chirality distribution of the CNTs in the bundle and the temperature.

This paper studies the electrical behavior of vias made by bundles of either SWCNTs or MWCNTs and proposes a simple and accurate equivalent lumped model, which includes in a self-consistent way the effects of size, temperature, chirality and frequency up to hundreds of gigahertz. The reference problem is depicted in Fig.1, where a pair of vertical interconnects is considered. The configuration can represent a pair of vias on-chip or a pair of chip-to-package interconnects like pillar bumps.

The electrical behavior of carbon nanotube interconnects in the low frequency regime can be described through a transmission line model ([8]-[9]). Beside the classical electromagnetic per-unit-length (*p.u.l.*) parameters, the carbon nanotube interconnect is characterized by the *p.u.l. kinetic inductance*, the *p.u.l. quantum capacitance* and the *p.u.l. resistance*, which strongly depends on the equivalent number of conducting channels. This parameter represents the average number of subbands in the neighbors of the CNT Fermi level that contribute to the axial conductivity of the carbon nanotube. It depends on the radius, chirality and temperature of the carbon nanotube [9]. Carbon nanotube vias are electrically short, thus they can be modeled as lumped elements (see figure 1d) [10]-[11].

Case-Study 1 refers to the configuration of Figure1, assuming $D = 1.26\mu\text{m}$, $H = 10D$, $d = 5.63\mu\text{m}$ and a total current flowing in the via of 0.301mA. We compare three realizations: (i) copper; (ii) SWCNT bundle, with $D = 6\text{ nm}$, and a fraction of 1/3 metallic CNTs; (iii) MWCNT, with outer and inner diameters $D_{out} = 100\text{ nm}$ and $D_{in} = 0.5D_{out}$ and a fraction of 1/3 metallic shells for each CNT.

Table I shows the computed values for the inductance L_v , comparing the Cu and CNT realizations. For the CNT realizations we have reported the value of the inductance where only the kinetic term is considered, and the value obtained taking also into account the magnetic term. The most relevant contribution is given by the kinetic inductance, which does not depend on frequency: for this reason CNT bundles are insensitive to skin-effect.

Case-Study 2, which is given by a pair of pillar bumps where the wire bond pitch d is $30\mu\text{m}$ and the pillar diameter is $D_b = 15\mu\text{m}$ whereas $l = 3D_b$. This is a very short vertical interconnect, for which it is of interest the

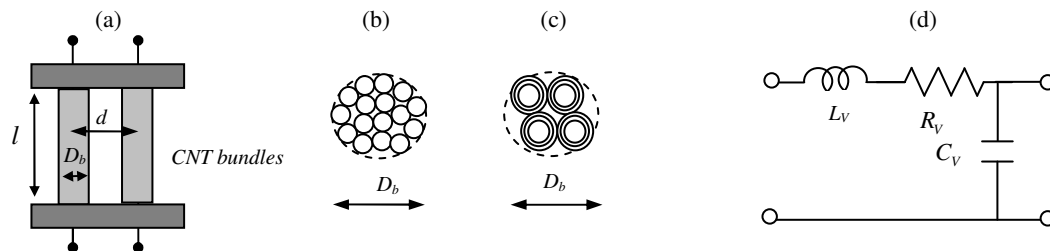


Figure 1. A pair of CNT-based vertical interconnects: (a) geometry; (b) SWCNT realization; (c) MWCNT realization, (d) equivalent circuit.

evaluation of the resistance. For the CNT bundle we assume the same conditions as for Case-study 1, unless for the CNT diameters, which are now 2 nm for SWCNTs and 100 nm for MWCNT (outer diameter). Table II reports the resistance values obtained for different frequencies and operating temperatures. The copper pillar pair exhibits a resistance strongly dependent on frequency and slightly dependent on temperature. The CNT realizations are insensitive to frequency, as seen also in the analysis of Case-Study 1. The SWCNT realization is much more sensitive to the increase of T than the MWCNT realization.

Figure 2 shows the *Temperature Coefficient of Resistance* (TCR) computed at $T=300\text{K}$, versus the interconnect length, assuming three different values of transverse characteristic dimension D_b (22, 44 and 100 nm), which are typical values for local, intermediate and global levels at 22nm node. For the CNT bundle realizations different possible values for the SWCNT and MWCNT diameters are considered. The TCR for copper is evaluated by using the model in [10] and it results to be constant with length and decreasing for decreasing D_b . For a SWCNT, TCR increases with length and decreases with D_b : however, increasing D_b results in a lower number of SWCNTs in the bundle, so in higher bundle resistance. The TCR for a MWCNT decreases with D_b increasing and increases with increasing length, and so the TCR may attain negative values.

TABLE I: INDUCTANCE IN [pH] OF THE VIAS FOR CASE-STUDY 1

f [GHz]	Cu	SWCNT (kinetic)	SWCNT (complete)	MWCNT (kinetic)	MWCNT (complete)
1	1.2599	23.6138	35.8377	29.0214	40.9606
10	1.2512	23.6138	35.8362	29.0214	40.9445
100	0.8534	23.6138	35.8162	29.0214	40.9427

TABLE II: RESISTANCE IN [m Ω] OF THE PILLARS (CASE-STUDY 2)

f [GHz]	Cu (300K)	Cu (400K)	SWCNT (300K)	SWCNT (400K)	MWCNT (300K)	MWCNT (400K)
1	9.60	11.36	22.27	49.42	6.44	14.67
10	27.41	32.13	22.27	49.42	6.44	14.67
100	83.95	97.88	22.27	49.42	6.44	14.67

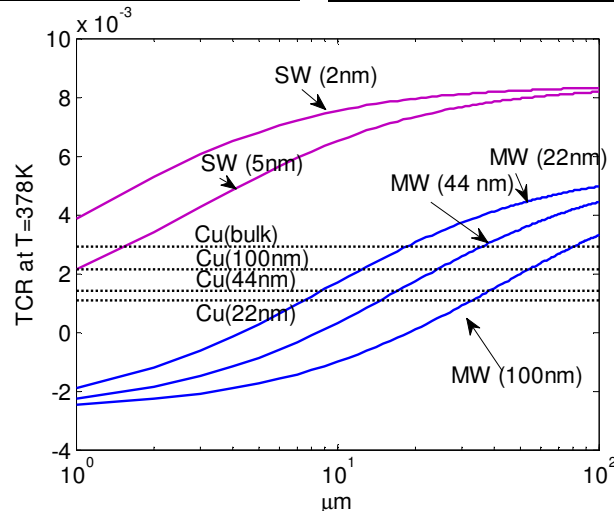


Figure 2. Temperature coefficient of the resistance at $T=378\text{K}$ versus wire length: Cu, SWCNT and MWCNT.

References

- [1] Ph. Avouris, Z. Chen, V. Perebeinos, "Carbon Based Electronics," *Nature Nanotechnology*, Vol 2, pp.605, 2007.
- [2] A. Naemi, J. D. Meindl, "Performance Modeling for Single- and Multiwall Carbon Nanotubes as Signal and Power Interconnects in Gigascale Systems," *IEEE Trans. on Electron Devices*, Vol. 55, n.10, pp. 2574-2582, Oct. 2008
- [3] A. Maffucci, G. Miano, F. Villone, "Performance Comparison Between Metallic Carbon Nanotube and Copper Nano-interconnects", *IEEE Trans. Advanced Packaging*, Vol.31, no.4, pp. 692-699, Nov 2008.
- [4] G. F. Close, S. Yasuda, B. Paul, S. Fujita and H.-S. Philip Wong, "A 1 GHz Integrated Circuit with Carbon Nanotube Interconnects and Silicon Transistors," *Nano Letters* vol.8, no.2, pp.706-709, 2009.
- [5] Soga I. *et al.*, "Carbon nanotube bumps for LSI interconnect," *Proc. of ECTC (2008)*, pp.1390-1394.
- [6] Xu, T.; Wang, Z.; Miao, J.; Chen, X. and Tan, C.M., "Aligned carbon nanotubes for through-wafer interconnects," *Appl. Phys. Lett.*, Vol. 91, pp. 042-108, 2007.
- [7] ITRS, International Technology Roadmap for Semiconductors, Edition 2009, <http://public.itrs.net>
- [8] A. Maffucci, G. Miano and F.Villone, "A transmission line model for metallic carbon nanotube interconnects," *Intern. J. of Circuit Theory and Applic.*, Vol. 36, no.1, pp.31, 2008.
- [9] G. Miano, C. Forestiere, A. Maffucci, S. A. Maksimenko, G.Y. Slepyan, "Signal propagation in single wall carbon nanotubes of arbitrary chirality," *IEEE Transactions on Nanotechnology*, Vol.10, pp. 135-149, 2011.
- [10] A.G. Chiariello, A. Maffucci, G. Miano, "Size and Temperature Effects on the Resistance of Copper and Carbon Nanotubes Nano-interconnects", *Proc. of IEEE EPEP 2010*, Austin, USA, pp. 97-100, 2010.
- [11] A.G. Chiariello, A. Maffucci, G. Miano, "Electrical Behaviour of Carbon Nanotube Through-Silicon Vias," *Proc. of IEEE SPI 2011*, pp.75-80, Naples, Italy, 8-11 May 2011.